CLAIMS

1. An insulated gate field effect transistor, comprising:

a semiconductor body (2) having opposed first (4) and second major surfaces (6);

a source region (14) of first conductivity type at the first major surface;

a body region (12) of second conductivity type opposite to the first conductivity type under the source region;

a drift region (10) of first conductivity type under the body region;

a drain region (8) of first conductivity type under the drift region, so that the source, body, drift and drain regions regions extend in that order from the first major surface towards the second major surface; and

insulated trenches (20) extending from the first major surface (4) towards the second major surface past the source region (14) and the body region (12) into the drift region (10), each trench (20) having sidewalls (22), and including insulator (28) on the sidewalls, at least one conductive gate electrode (32) adjacent to the body region (12) separated from the body region (12) by a gate insulator (42), and at least one conductive field plate electrode adjacent to the drift region separated from the drift region by a field plate insulator (44), and a gate-field plate insulator (30) separating the field plate from the gate,

wherein the source regions (14) and trenches (20) define a pattern of cells across the first major surface; and

the doping concentration in the drift region (10) increases from the part of the drift region (10) adjacent to the body region (12) to the part of the drift region (10) adjacent to the drain region (12), the doping concentration in the drift region (10) being at least 50 times greater adjacent to the drain region (8) than adjacent to the body region (12).

2. An insulated gate field effect transistor according to claim 1 in which the gate electrode (32) is of conductive semiconductor doped to be the second conductivity type.

3. An insulated gate field effect transistor according to any preceding claim wherein the gate electrode (32) has side pieces (50) spaced apart adjacent to the sidewalls (22) on either side of the trench and a top piece (52) spanning the gap between the side pieces.

4. An insulated gate field effect transistor according to any preceding claim wherein the breakdown voltage is less than or equal to 30V.

5. An insulated gate field effect transistor according to any preceding claim wherein the pattern of cells (40) defined by the source regions (14) and trenches (20) arranged across the first major surface is a pattern in which cells (40) repeat in more than one direction across the surface to form a three-dimensional cell structure.

6. An insulated gate field effect transistor according to claim 5 wherein the cells (40) are arranged in a hexagonal pattern.

7. An insulated gate field effect transistor according to any preceding claim further comprising a trench (62) filled with conductive material extending through the source region (14) to the body region (12) to connect the source contact (16) to the source region (14) and the body region (12).

8. An insulated gate field effect transistor according to claim 7 further comprising a doped contact region (60) of second conductivity type in the body region in contact with the conductive material in the trench (62), the doping concentration in the doped contact region (60) being higher than the doping in the rest of the body region (12).

9. An insulated gate field effect transistor according to any preceding claim wherein the thickness of the insulator thickness adjacent to

the field plate electrode (34) is greater than the thickness of the insulator adjacent to the gate electrode (32).

10. An insulated gate field effect transistor according to any preceding claim wherein the cell pitch is not greater than 1 micron.

11. An insulated gate field effect transistor according to any preceding claim wherein the first conductivity type is n-type, the second conductivity type is p-type and the gate is of p-type doped polysilicon.

12. An insulated gate field effect transistor according to any preceding claim wherein the field plate oxide (44) thickness is in the range 0.6 to 1 micron and the gate oxide (28) thickness is in the range 0.2 to 0.5 micron.

13. An insulated gate field effect transistor according to any preceding claim wherein the field plate electrode (34) is connected to the source (14).

14 An insulated gate field effect transistor according to any of claims 1 to 12 further comprising a field plate terminal (38) connected to the field plate (34) for controlling the field plate voltage independently.